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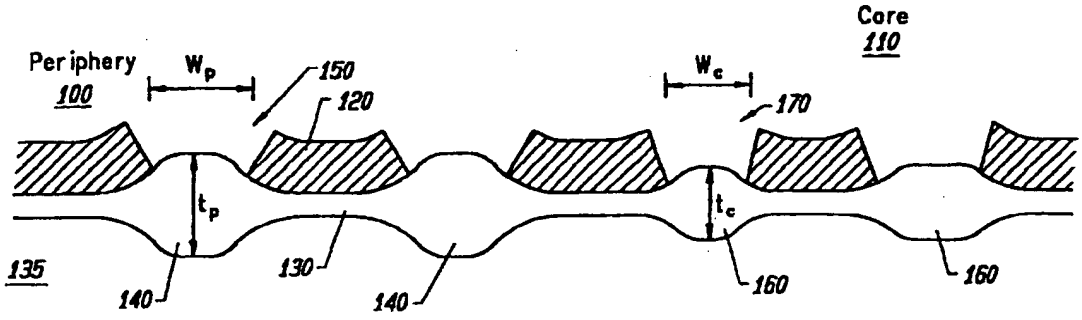

(57) Abstract

A local oxidation of silicon (LOCOS) process directed to forming differential field oxide thickness on a single wafer in one patterning step and one growth step. When patterning the masking layer, at least two window widths are formed in the masking layer, exposing the underlying substrate and pad oxide. When one of the window widths is sufficiently small, oxidation of the substrate will be inhibited causing reduced growth and thus a reduced field oxide thickness in that window as compared to other larger windows formed in the same masking layer, creating differential field oxide thicknesses in one growth step.

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METHOD FOR DIFFERENTIAL FIELDOX GROWTH

BACKGROUND OF THE INVENTION

1. Field of Invention

The invention relates to local oxidation of silicon (LOCOS) processes and more particularly to differential field oxide growth on a single wafer.

2. Description of Related Art

Generally, in integrated circuit devices, active devices are formed on a semiconductor substrate. In integrated circuits such as memories, programmable logic devices (PLDs), and other integrated circuits, active devices must be electrically isolated from each other. One way to isolate the devices is to grow a field oxide region between devices, as shown in Fig. 1, typically through a local oxidation of silicon (LOCOS) process.

LOCOS processes typically begin with a silicon substrate upon which is grown a thin pad oxide (typically 100Å-500Å). A nitride (Si_xN_y) layer is deposited over the pad oxide. The nitride layer is patterned and parts are removed to form windows exposing the pad oxide. The resulting structure is shown in the cross-section of Fig. 2A. Occasionally some or all of that portion of the pad oxide underlying the removed nitride portion is also removed exposing the substrate. The wafer is then exposed to an oxidizing ambient, either a wet or dry oxidant, and oxidation of the exposed substrate and pad oxide takes place. The result, shown in Fig. 2B, is a field oxide region that effectively isolates neighboring devices (transistors) from one another. Note that a pad oxide is not necessary for oxidation but is beneficial in relieving stress that occurs.

As shown in the cross-section of Fig. 2B, during the oxidation, the field oxide region not only grows vertically, up into the window formed by the patterned nitride and directly below the window into the substrate, but the oxidant also diffuses laterally, under the nitride. This lateral diffusion is known as encroachment (ΔW) and forms an area in the field oxide known as the "bird's beak." Encroachment is typically undesirable as it causes a larger field oxide area than is desired, thus decreasing packing density of devices per wafer. Because as field oxide thickness increases, encroachment also increases, one way to minimize encroachment is to use the minimum field oxide thickness required.

Memory devices can typically be divided into core and periphery regions, shown in the block diagram of Fig. 3. The core region 110 contains specialized memory cells which are used solely for information storage, while the periphery region 100 contains various logic needed to make stored information accessible, making the two regions functionally distinct. Such center versus edge placement is typical, however, but not required of memory cell structure.

Typically, during fabrication of memory cells, manufacturers grow field oxide regions of the same thickness in both the core and the periphery, usually approximately 4000Å. However, due to device considerations, e.g., voltages, doping, and field thresholds, only an isolation region of approximately 2500Å is needed between devices in the core compared with that required for the periphery. In addition, use of a smaller isolation region in the core decreases the amount of encroachment experienced in the core and would allow increased packing density for memory cells thereby allowing memory chips to either shrink in size or to increase storage capacity on the same size chip. Thus, it is desirable to grow field oxides of different thicknesses on a single substrate.

SUMMARY OF THE INVENTION

The present invention, roughly described, is directed toward a method for differential field oxide growth. It is desirable on some integrated circuits, and particularly memory devices, that the isolation, or field oxide, regions be of different thicknesses in the core area and the periphery area of the device. However, it is further desirable to be able to achieve differential field oxide growth using only one patterning step and one growth step.

The process used to achieve differential field oxide growth in one patterning step and one growth step begins with a silicon substrate upon which is formed a pad oxide layer and a masking layer. Portions of the masking layer are removed to form "windows" in the masking layer. The window width in the core is smaller than the window width in the periphery. Use of the smaller window in the core takes advantage of the "field thinning effect."

According to the "field thinning effect," when the window width is smaller than a particular width specific to each oxidation process, oxidation will be significantly inhibited causing a smaller field oxide thickness to be grown than if the window width were larger. Thus, by patterning different sized windows in the core and periphery, different field oxide thicknesses can be grown in a single growth step.

The process in accordance with the invention is advantageous in that it improves packing density of devices per wafer because smaller field oxide thicknesses will be used when larger field oxide thicknesses are not required.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described with respect to particular embodiments thereof, and reference will be made to the drawings in which:

Fig. 1 is a cross-sectional view of a wafer construct having isolation regions;

Fig. 2A is a cross-sectional view of wafer construct prior to a conventional LOCOS process;

Fig. 2B is a cross-sectional view of the wafer construct immediately subsequent to oxidation in a conventional LOCOS process;

Fig. 3 is a representational block diagram of a memory device;

Fig. 4A shows a cross-sectional view of a wafer construct following the first step of one method for developing a wafer construct having differential field oxide thicknesses;

Fig. 4B is a cross-sectional view of a wafer construct following the second step in one method of forming a wafer construct having differential field oxide thicknesses;

Fig. 5 is a generic characteristic curve of an oxidation process, showing nitride spacing to field oxide thickness;

Fig. 6 is a cross-sectional view of a wafer construct resulting from one embodiment of the present invention;

Fig. 7 is shows the characteristic curves of nitride spacing to field oxide thickness for a dry oxidation process and for a wet oxidation process;

Fig. 8A shows a cross-sectional view of a wafer construct using spacers and trenching resulting from one embodiment of the present invention immediately prior to oxidation;

Fig. 8B is a cross-sectional view of the wafer construct resulting from the process according to one embodiment of the present invention.

DETAILED DESCRIPTION

Due to individual device considerations, e.g., voltages, doping, field thresholds, devices on many integrated circuits do not require that the isolation regions between devices on the integrated circuit be the same thickness. For instance, in memory devices, the isolation regions in the core 110 can be significantly smaller in thickness (e.g.,

2500Å) than the isolation regions in the periphery 100 (e.g., 4000Å). By growing only the smallest isolation region necessary for effective isolation of devices, space on the wafer can be optimized and conserved.

One way to achieve dual field oxide thicknesses, one thickness in the core area 110 and one thickness in the periphery area 100, is to grow the field oxide in two steps: first, as shown in Fig. 4A, patterning the nitride in the periphery to form windows with width W_p and growing a partial thickness in the periphery while the core remains completely covered with nitride; and second, as shown in Fig. 4B, patterning the core to form windows with width W_c equal to width W_p and growing the field oxide in the core to t_c while the field oxide in the periphery continues growing to its final thickness of t_p. However, while this method accomplishes the goal of having dual field oxide thicknesses, it requires two patterning steps and two field oxide growths.

Thus, it is desirable to grow field oxide regions of different thicknesses on a single substrate using only a single patterning step and a single growth step. Therefore, in accordance with the invention, another way to accomplish differential field oxide growth is to take advantage of the "field thinning effect," which is characterized in Fig. 5. Under this effect, the thickness t of the field oxide grown depends upon the width of the "windows" 150 and 170 in nitride layer 120 (Fig. 6). As the window closes, the supply of oxygen to the substrate is reduced. While the magnitude and details of the field thinning effect will depend on the specifics of each oxidation cycle, e.g., time, temperature and ambient, and must be mapped for each oxidation cycle, the nitride spacing to field oxide thickness curve will generally appear as shown in Fig. 5 for most oxidation processes.

Once the field oxide thicknesses desired for a particular device are determined, reference is made to the characteristic curve of the oxidation process generically shown in Fig. 5. By tracing a line horizontally from a thickness t to the curve and then from the curve vertically down, a determination of window width w can be made for thickness t. The nitride is then etched to pattern the surface with the various window widths determined from the characteristic curve, e.g., W_p and W_c, as shown in Fig. 6. Note that the portion of the pad oxide 130 underlying the removed nitride portions may also be completely or partially removed in this etch step in one embodiment of the invention.

Oxidation of the exposed regions can then take place growing oxides to a thickness t_p in the periphery and t_c in the core. If W_c is

found from the curve of Fig. 5 in the area where the curve "rolls off," and W_p is taken from that part of the curve that is relatively flat, then, once oxidized, the resulting t_c will be smaller than the resulting t_p, as shown in Fig. 6. Thus, only one patterning step and one field oxide growth is required.

Fig. 7 shows curves for a dry oxide process at 1125°C as well as a wet oxide process at 1000°C. Note that the "rolloff" shown on these curves has conventionally been thought of as undesirable and most LOCOS processes avoid "windows" falling in the "rolloff" region. For the wet oxidation process at 1000°C shown by curve 710, significant reductions in field oxide thickness occur when nitride spacing is below a width of one micron. However, for the dry oxidation process shown by curve 720, significant reductions occur in field oxide thickness at a window spacing of 0.4 microns and below. While either a wet oxidation process or a dry oxidation process can be used in alternative embodiments of the invention, because of the gradual sloping of the wet oxidation curve 710 from a width of one micron, it is likely that significant amounts of space on the substrate wafer will have to be sacrificed to achieve the same results as the dry oxidation process 720.

The dry oxidation process used in one embodiment of the invention is a multi-step oxidation process, in which a first oxidation step is performed at a temperature of approximately 1000°C in an atmosphere comprising approximately 0.1-10% HCl and 90-99.9% O_2 for a period of approximately 30 to 120 minutes. This first oxidation step forms a thin oxide layer over nitride 120 to protect the nitride from reacting with HCl during the later oxidation steps. The reaction of nitride 120 with HCl is dependent on temperature and does not occur below approximately 1050°C. The purpose of adding HCl to the oxidizing atmosphere for the first oxidation step is to clean the surface to be oxidized by removing, for example, metallic contamination.

A second oxidation step is performed at a temperature of approximately 1125°C in an atmosphere comprising approximately 0.1-10% HCl and 90-99.9% O_2 for a period of approximately 4 to 10 hours. As in the first oxidation step the concentrations of HCl and O_2 in the oxidizing environment may be optimized by those of ordinary skill in the art. HCl is added to the oxidizing environment in the second oxidation step to prevent stacking faults. It is believed that O_2 is injected into the crystalline lattice of silicon substrate 135 and that this interstitial O_2 causes mismatches in the lattice which lead to stacking faults. The HCl neutralizes the interstitial O_2, thereby preventing stacking faults.

Both oxidation steps include a stabilization period in an inert or oxidizing atmosphere. In the multi-step oxidation embodiment of the invention the atmosphere for the stabilization period of the first oxidation step comprises 10-40% O_2 and 60-90% Argon and the atmosphere for the stabilization period of the second oxidation step comprises approximately 100% Argon. Those of ordinary skill in the art will be able to optimize the atmosphere during the stabilization period. Further details regarding this oxidation process can be found in *Liu*, et al., U.S. Patent No. 5,151,381, incorporated by reference herein.

Thus, a process has been described for forming field oxide regions of differing thicknesses in one patterning step and one growth step (the growth step in the embodiment described above includes two oxidation steps). Other embodiments are described below.

In another embodiment of the invention spacers are used to decrease the window size in the nitride. In such an embodiment the nitride layer would be patterned and etched in the core region. Then a spacer forming material, typically nitride, would be deposited over the patterned wafer, and then etched anisotropically to form spacers in the core. The nitride layer could then be patterned and etched in the periphery to form windows equal in width to those formed in the core prior to spacer formation. Field oxide growth could then occur in a single growth step. While this embodiment adds extra steps compared to other embodiments of the invention, such spacers could be useful in lithographically limited situations.

In another embodiment of the invention substrate trenching is used to further improve the planarity of the field oxide. Figs. 8A and 8B show an embodiment of the invention using both spacer formation and substrate trenching. Fig. 8A shows the wafer structure prior to oxidation having spacers 175 positioned within window 170 and abutting nitride layer 120 and having a trench 180 etched within substrate 135. Fig. 8B shows the structure subsequent to oxidation with field oxide region 160. Nitride spacers 125 on the sides of the original nitride stack may further improve encroachment ΔW by approximately the width of the spacer 175. Trenching 180, while trading back some of the ΔW gained with the spacers, may be used to improve resulting planarity. In each of the embodiments described above, the characteristic nitride spacing to field oxide thickness curve will vary between embodiments.

It should be understood that the particular embodiments described above are only illustrative of the principles of the present invention, and various modifications could be made by those skilled in the art without departing from the scope and spirit of the invention. For instance, while the invention has been described in the context of a

memory device, it is to be understood that the process according to the invention could also be used in developing PLD's or other integrated circuits and devices where differential field oxide thicknesses are desired. Thus, the scope of the present invention is limited only by the claims that follow.

CLAIMS

What is claimed is:

1. A method of forming isolation regions on a substrate, comprising the steps of:

forming a pad oxide layer over said substrate;

forming a masking layer over said pad oxide layer;

forming a first window having a first width in said masking layer;

forming a second window having a second width in said masking layer; and

forming a first isolation region of a first thickness extending into said first window and forming a second isolation region of a second thickness extending into said second window.

2. The method of claim 1, wherein said step of forming a first isolation region and forming a second isolation region includes exposing said substrate to an oxidizing ambient.

3. The method of claim 1, wherein said step of forming said first window includes forming said first window in said masking layer having said first width of less than approximately 0.4 microns, and said step of forming said second window includes forming said second window in said masking layer having said second width of more than approximately 0.4 microns.

4. The method of claim 1, wherein said step of forming a first isolation region and forming a second isolation region includes forming a first isolation region having a thickness of approximately 2500Å and forming a second isolation region having a thickness of approximately 4000Å.

5. The method of claim 1, further comprising the steps, preceding said steps of forming said first window and forming said second window, of:

determining a mask window width to field oxide thickness curve for an oxidation process;

using said curve, determining said first mask window width corresponding to said first thickness; and

using said curve, determining said second mask window width corresponding to said second thickness.

6. The method of claim 1, wherein said step of forming a first window includes:

forming a window having a width greater than said first width;

forming spacers within said window.

7. A method of forming field oxide regions on a semiconductor substrate, comprising the steps of:

forming a pad oxide layer over said substrate;

forming a nitride layer over said pad oxide layer;

determining a mask window width to field oxide thickness curve for an oxidation process;

using said curve, determining a first mask window width corresponding to a first field oxide thickness;

using said curve, determining a second mask window width corresponding to a second field oxide thickness;

etching a first window in said masking layer, said first window having a width approximately equal to said first mask window width;

etching a second window in said masking layer, said second window having a width approximately equal to said second mask window width; and

forming a first field oxide region of said first field oxide thickness extending into said first window and forming a second field oxide region of said second field oxide thickness extending into said second window.

8. The method of claim 7, wherein said step of forming a first field oxide region and forming a second field oxide region includes oxidizing said substrate using said oxidation process.

9. The method of claim 7, wherein said step of forming a first field oxide region and forming a second field oxide region includes growing a first field oxide region having a thickness of approximately 2500Å and growing a second field oxide region having a thickness of approximately 4000Å.

10. The method of claim 7, wherein:

said step of forming a first window in said masking layer includes forming said first window having a width of less than approximately 0.4 microns; and

said step of forming a second window in said masking layer includes forming said second window having a width of more than approximately 0.4 microns.

11. The method of claim 7, wherein said step of forming a first window includes:

forming a window having a greater width than said first mask window width; and

forming spacers within said window.

12. The method of claim 9, wherein said substrate has a core region and a periphery region, and wherein: said first field oxide region is located in the core region; and

said second field oxide region is located in the periphery.

13. The method of claim 8, wherein said step of oxidizing said substrate includes exposing said substrate to an oxidizing ambient at a temperature of approximately 800°C to 1200°C.

14. The method of claim 13, wherein said step of oxidizing said substrate includes exposing said substrate to a dry oxide at a temperature of approximately 1125°C.

15. A structure comprising;

a substrate;

a pad oxide layer over said substrate;

a masking layer over said pad oxide layer, said masking layer having a first window of a first width and a second window of a second width; and

a first isolation region of a first thickness extending into said first window; and

a second isolation region of a second thickness extending into said second window.

16. The structure of claim 15, wherein:

said first thickness is smaller than said second thickness; and

said first width is smaller than said second width.

17. The structure of claim 16, wherein:

said first thickness is approximately 2500Å and said second thickness is approximately 4000Å; and

said first width is less than approximately 0.4 microns and said second width is more than approximately 0.4 microns.

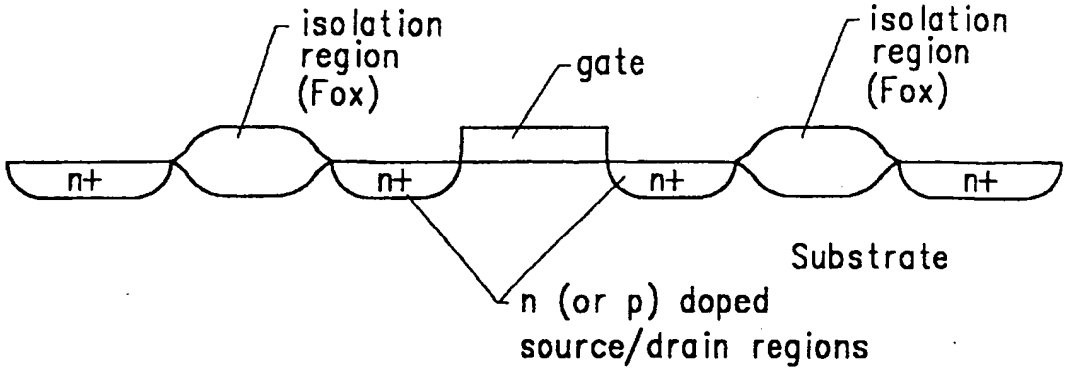


FIG. 1

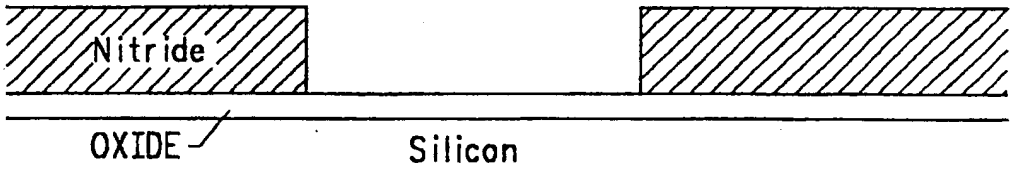


FIG. 2A

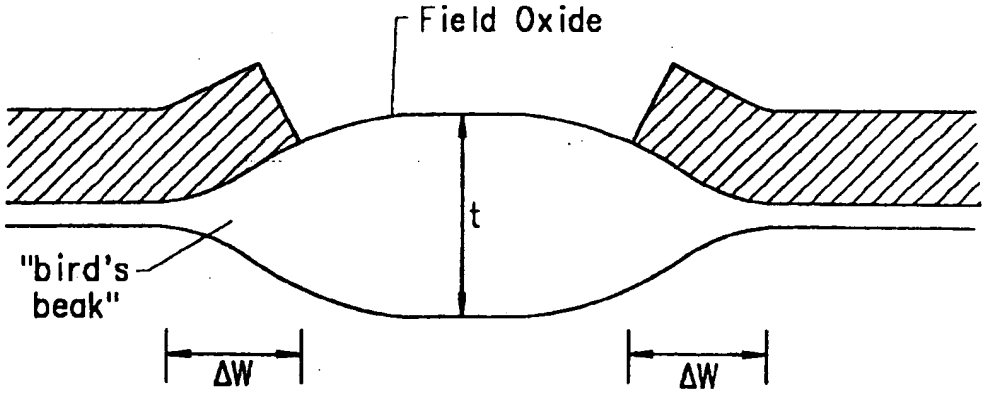


FIG. 2B

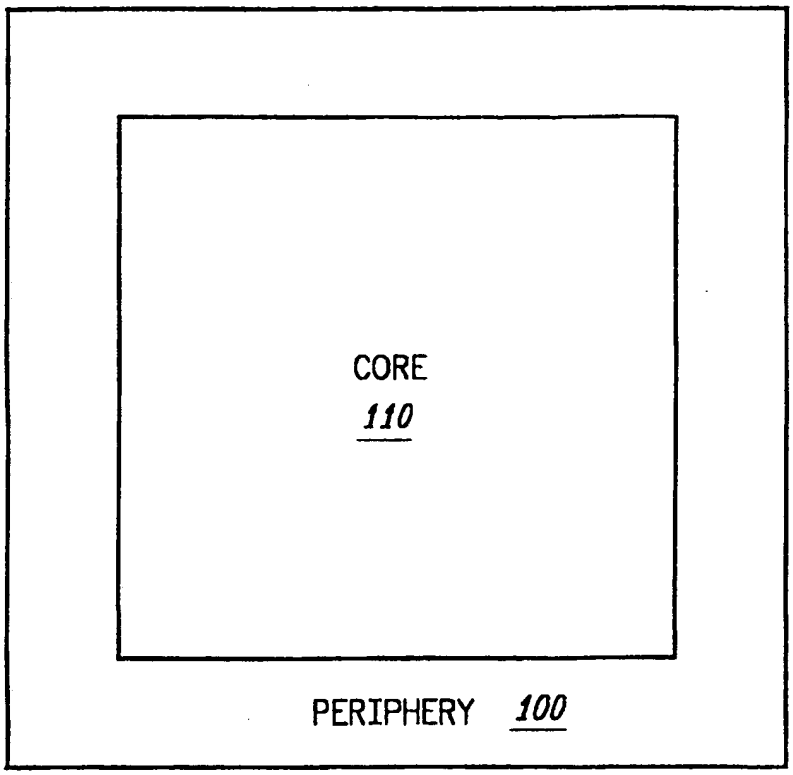
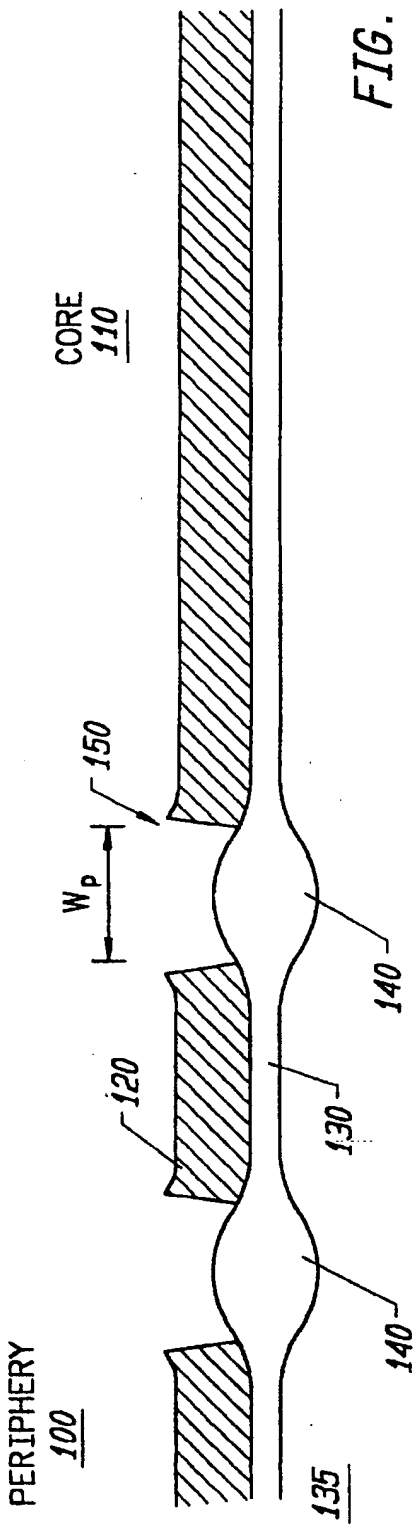


FIG. 3


PERIPHERY
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CORE
110
150
W_p
120
130
140
140
135

FIG. 4A

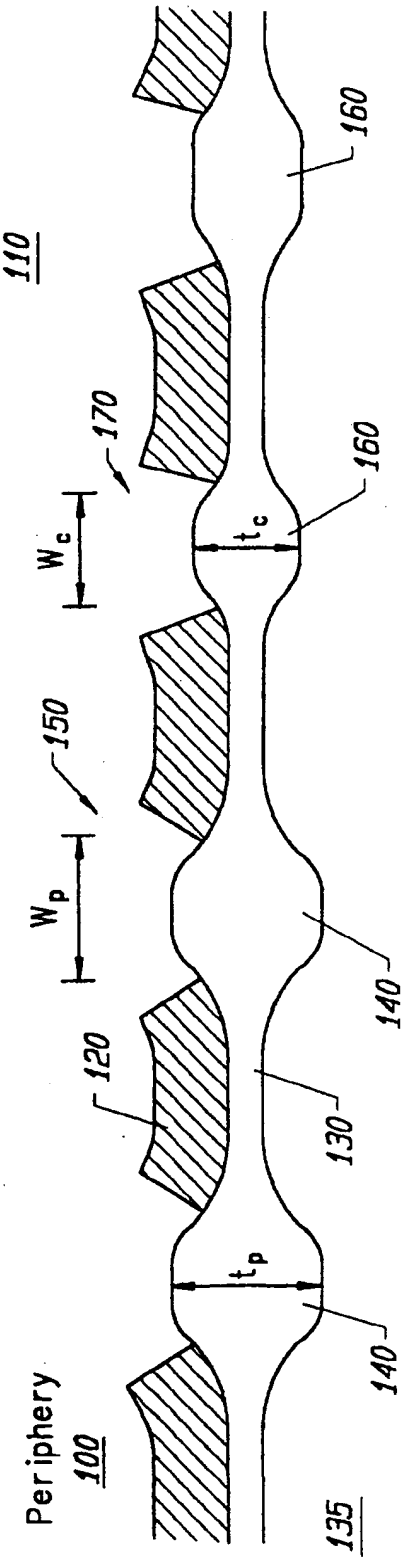
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FIG. 4B

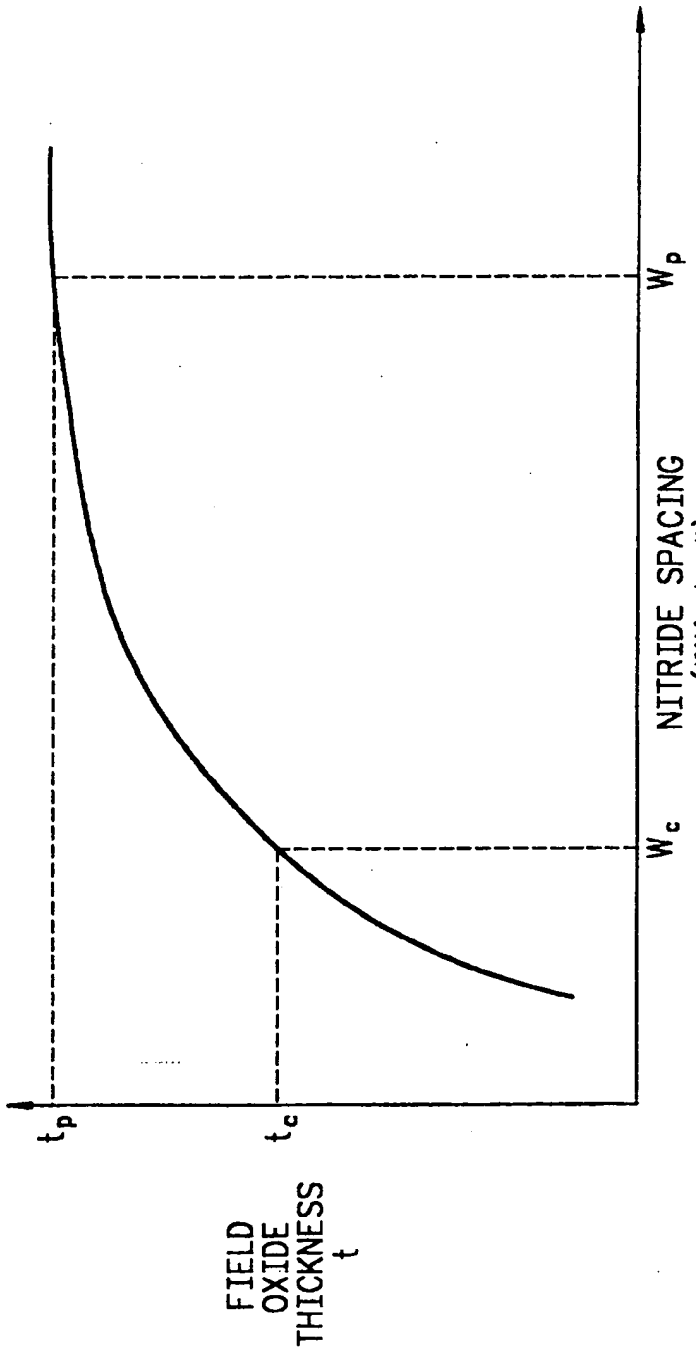
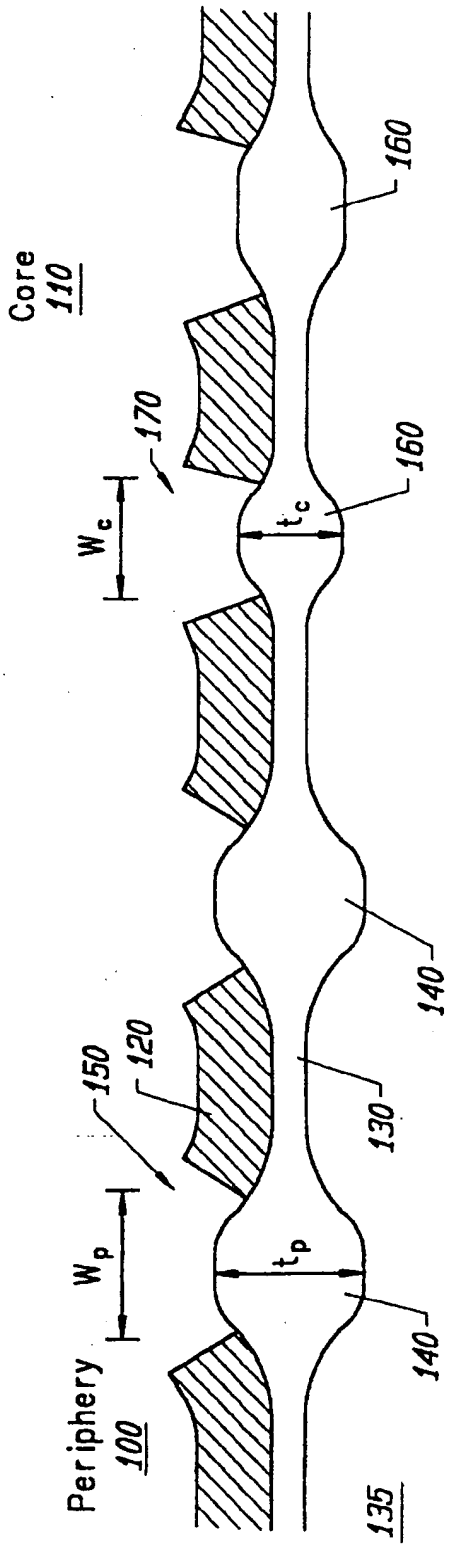


FIG. 5


Core
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Periphery
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130
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W_p
t_p

FIG. 6

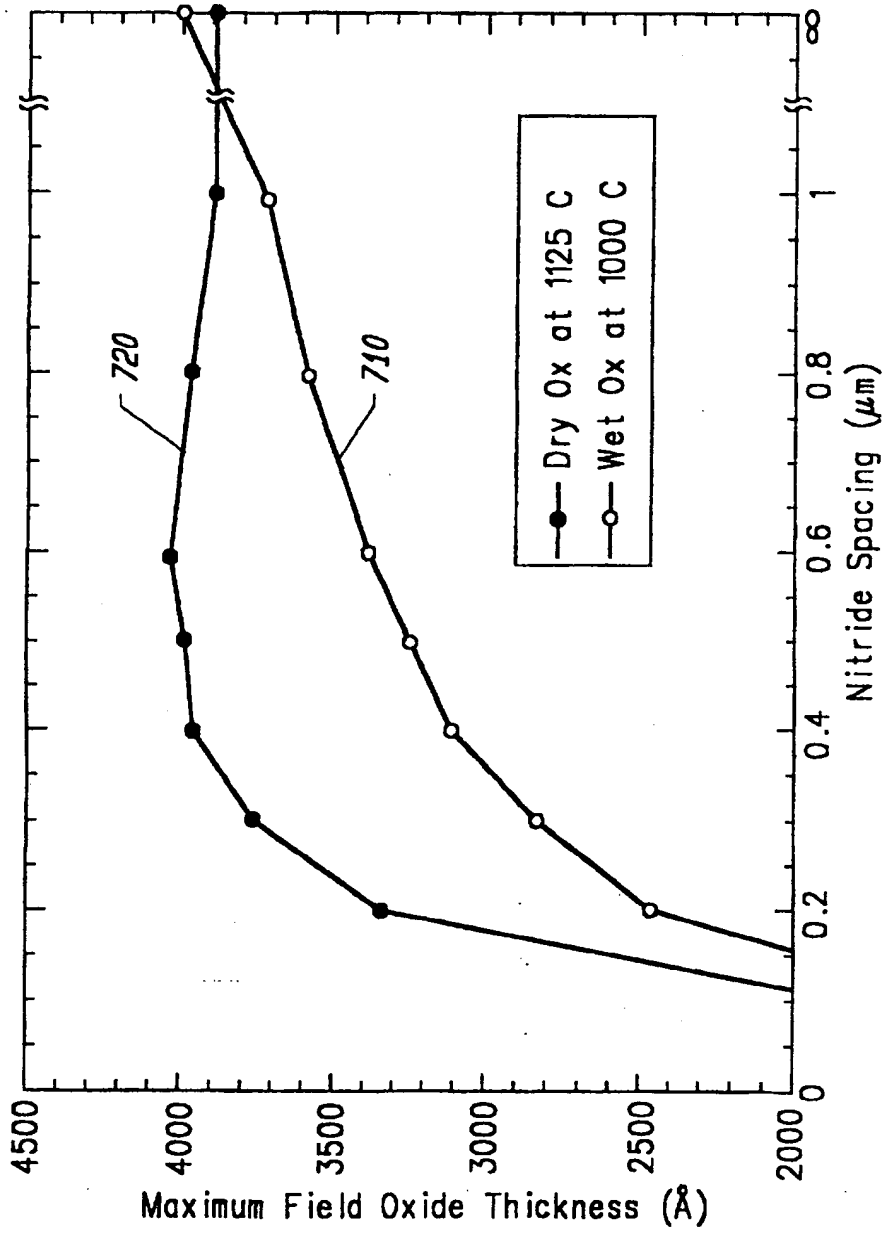
Dry Ox at 1125 C
Wet Ox at 1000 C
720
710
Maximum Field Oxide Thickness (Å)
4500
4000
3500
3000
2500
2000
Nitride Spacing (μm)
0
0.2
0.4
0.6
0.8
1

FIG. 7

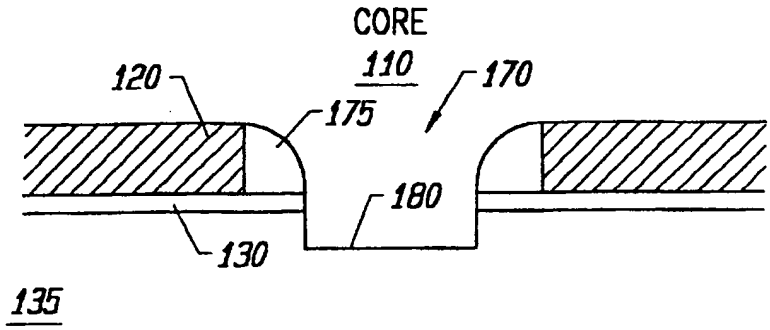

FIG. 8A

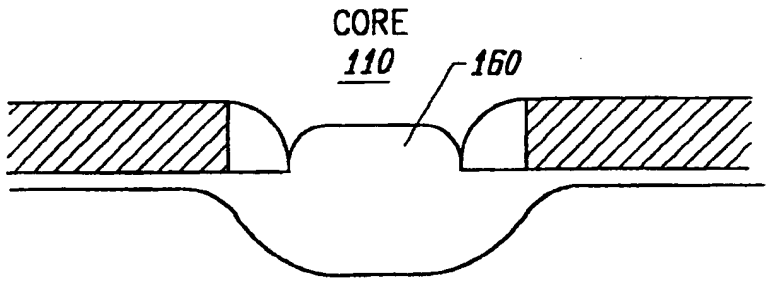

FIG. 8B

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/762 H01L21/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 08 172 087 A (GOLDSTAR ELECTRON CO LTD) 2 July 1996 & US 5 646 052 A (LEE CHANG JAE) 8 July 1997 see abstract; claim 1; figures 4,6A-C,12,13 see column 6, line 20 - line 39 see column 8, line 5 - line 62	1-5, 7-10,13, 15-17
Y	---	7,9,12
Y	PATENT ABSTRACTS OF JAPAN vol. 096, no. 006, 28 June 1996 & JP 08 055845 A (FUJITSU LTD), 27 February 1996, see abstract	7,9,12

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[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
18 December 1997	30/12/1997

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Wirner, C

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